REMARKS

Summary of Office Action

Claims 1-5, 15-18, and 29-32 were rejected under 35 U.S.C. § 102(e) as being anticipated by Camilleri et al. U.S. Patent No. 6,434,642 (hereinafter "Camilleri").

Claims 6-14 and 33-35 were objected to as being dependent upon a rejected based claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 19-28 were objected due to informalities in claim 19, but were indicated to be allowable if rewritten to overcome the claim objection.

Summary of Applicants' Response

Applicants note that claim 19 has already been amended to correct for the claim informalities in a Preliminary Amendment filed on January 16, 2001. Applicants respectfully submit that the Preliminary Amendment places claim 19, and claims 20-28 which depend there from, in condition for allowance.

Applicants note with appreciation the indication of allowable subject matter in claims 6-14 and 33-35. Applicants hereby expressly reserve the right to these claims in independent form, to the extent applicants have not already done so, if the base claims are ultimately not allowed.

Applicants respectfully traverse the rejections under 35 U.S.C. § 102(e).

Reply to Rejections Under 35 U.S.C. § 102(e)

Applicants respectfully submit that Camilleri fails to disclose, teach, or suggest the claimed invention.

Camilleri discloses a structure and method for operating a FIFO memory system with a "512x8 dual-port FIFO RAM 101" (col. 4, lines 63-64), "9-bit write address counter 103" (col. 4, lines 64-65), "9-bit read address counter 105" (col. 4, lines 65-66), "flag control circuit 107" (col. 4, lines 67-68) "for generating FULL and EMPTY" (col. 3, lines 18-19) signals in response to the outputs of the counters, and a status circuit "for generating a FIFO status signal indicating the amount of data stored in the FIFO memory at a given moment during operation" (col. 3, lines 20-22). The write address and read address counters "are consistent with conventional circular binary counters" (col. 5, lines 38-39) and generate addresses "that change in accordance with a predetermined circular binary counting sequence" (col. 3, lines 25-26).

As described in Camilleri, the flag control circuit generates the FULL and EMPTY signals to determine whether the memory is full or empty thereby preventing writing to or reading from the memory, respectively (col. 1, lines 37-47). Writing to or reading from the memory requires the FULL and EMPTY signals, read and write clocks as well as external "WRITE_ENABLE" and "READ_ENABLE" signals (FIG. 1). The FULL and EMPTY signals are generated "by converting the currently-generated binary read and write address signals into Gray-code address values, and then comparing the Gray-code address values to determine whether memory 101" (col. 5, lines 54-57) is full or empty. As described in Camilleri with reference to FIG. 2,

this requires flag control circuit 107 to be implemented with a current read address register (210), a last read address register (216), a current write address register (224), a comparator (230), and two binary-to-Gray code converters (222).

In contrast, the FIFO memory circuitry disclosed in the present invention requires much less complex circuitry; the memory is implemented with "Gray code counter circuitries" (counters 20 and 30, FIG. 1) to count the read and write clocks, a "Gray code subtractor circuitry" (40) to subtract the outputs of the counters and produce a Gray code output, and a "shift register circuitry" (60) that shifts successive data words in synchronism with the write clock and selects one of the data words based on the Gray code output generated by the subtractor. Reading to or writing from the memory simply requires the read and write clocks and the subtractor output, which may also be monitored to detect full or empty conditions of the shift register circuitry. As described in the specification, "by using Gray code in this manner, a FIFO memory can be provided which has reliable and glitch-free full, empty, and data output signals. The circuitry can be readily implemented in appropriately constructed programmable logic devices ("PLDs"), e.g., PLDs that include Gray code shift register capabilities" (page 3, lines 2-8).

Unlike the FIFO memory system in Camilleri, the FIFO memory of the present invention does not require external "WRITE_ENABLE" and "READ_ENABLE" signals for its operation, nor does it require binary-to-Gray code converters for generating Gray code outputs indicative of the status of the memory. The FIFO memory circuitry disclosed in the present invention is

implemented with 5 simple circuit components (FIG. 1) while the FIFO memory system disclosed in Camilleri requires 6 circuit components just to implement its flag control circuitry, in addition to the two circular counters, FIFO RAM, and status control circuit shown in FIG. 1. By using conventional circular binary counters, binary-to-Gray code converters and more complicated circuitry to implement a FIFO memory, Camilleri directly teaches away from using the Gray code counters and the simple shift registers as disclosed in the present invention.

The Examiner points to the abstract and FIG. 1 of Camilleri as disclosing the Gray code subtractor circuit and shift register circuitry of the present invention. Applicants respectfully disagree. FIG. 1 shows flag control circuit 107 being implemented, as described above, with read and write address registers, binary-to-Gray code converters, and a comparator. Nowhere in FIG. 1 is shown a subtractor circuit that processes the outputs of Gray code counters "to produce a Gray code output which is used to address shift register circuitry for reading" (page 2, lines 26-29).

First, there are no Gray code counters disclosed in Camilleri, but, rather, circular counters that are used with binary-to-Gray code converters for generating Gray code outputs. Second, the Gray code outputs of the circular counters/binary-to-Gray code converters combination are not sent to a subtractor circuit "to produce a Gray code output which is used to address shift register circuitry for reading" (page 2, lines 26-29). Instead, the Gray code outputs of the circular counters/binary-to-Gray code converters combination

are sent to a comparator that generates FULL and EMPTY signals that are used not to address a shift register but as indications of whether the memory is full or empty.

And lastly, the subtractor circuit pointed out by the Examiner in the abstract is a subtractor circuit included in "optional status control circuit 109" (col. 4, line 68) for generating a "FIFO_STATUS control signal that indicates the amount of data currently stored in the FIFO memory" (col. 20, lines 27-29). This control signal is a status signal that, similar to the FULL and EMPTY signals generated by flag control circuit 107, is not used to address a shift register as disclosed in the present invention.

Therefore, applicants respectfully submit that Camilleri does not disclose, teach, or suggest the claimed invention. In fact, by implementing a FIFO memory circuitry as described, Camilleri directly teaches away from the simple and efficient implementation disclosed in the present invention requiring just two Gray code counter circuitries, a subtractor circuitry, and a shift register circuitry.

Accordingly, applicants respectfully submit that Camilleri does not anticipate claims 1, 19, and 29 or claims 2-18, 20-28, and 30-35 which depend there from. Since Camilleri fails to anticipate the claimed inventions of claims 1, 19, and 29, applicants respectfully submit that claims 1, 19, and 29 and their respective dependent claims, distinguish from, and are allowable over, the cited reference.

Conclusion

Applicants respectfully submit that claims 1-35 are in condition for allowance, and respectfully request the same.

Respectfully submitted,

Daniel M. Becker
Registration No. 38,376

For: Robert R. Jackson
Reg. No. 26,183
Attorney for Applicants

FISH & NEAVE
1251 Avenue of the Americas
New York, New York 10020
Tel.: (650) 617-4000
FAX: (212) 596-9090